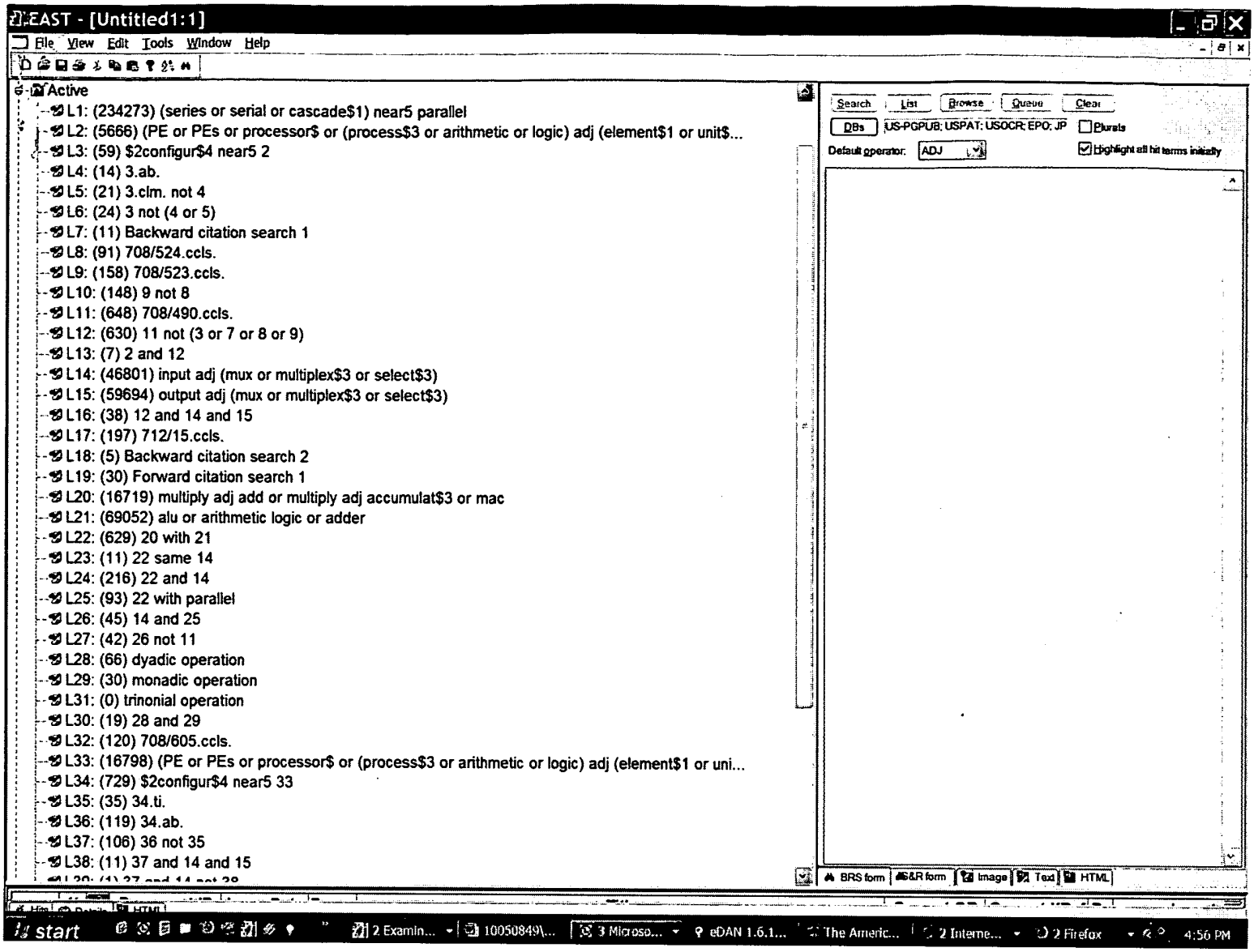

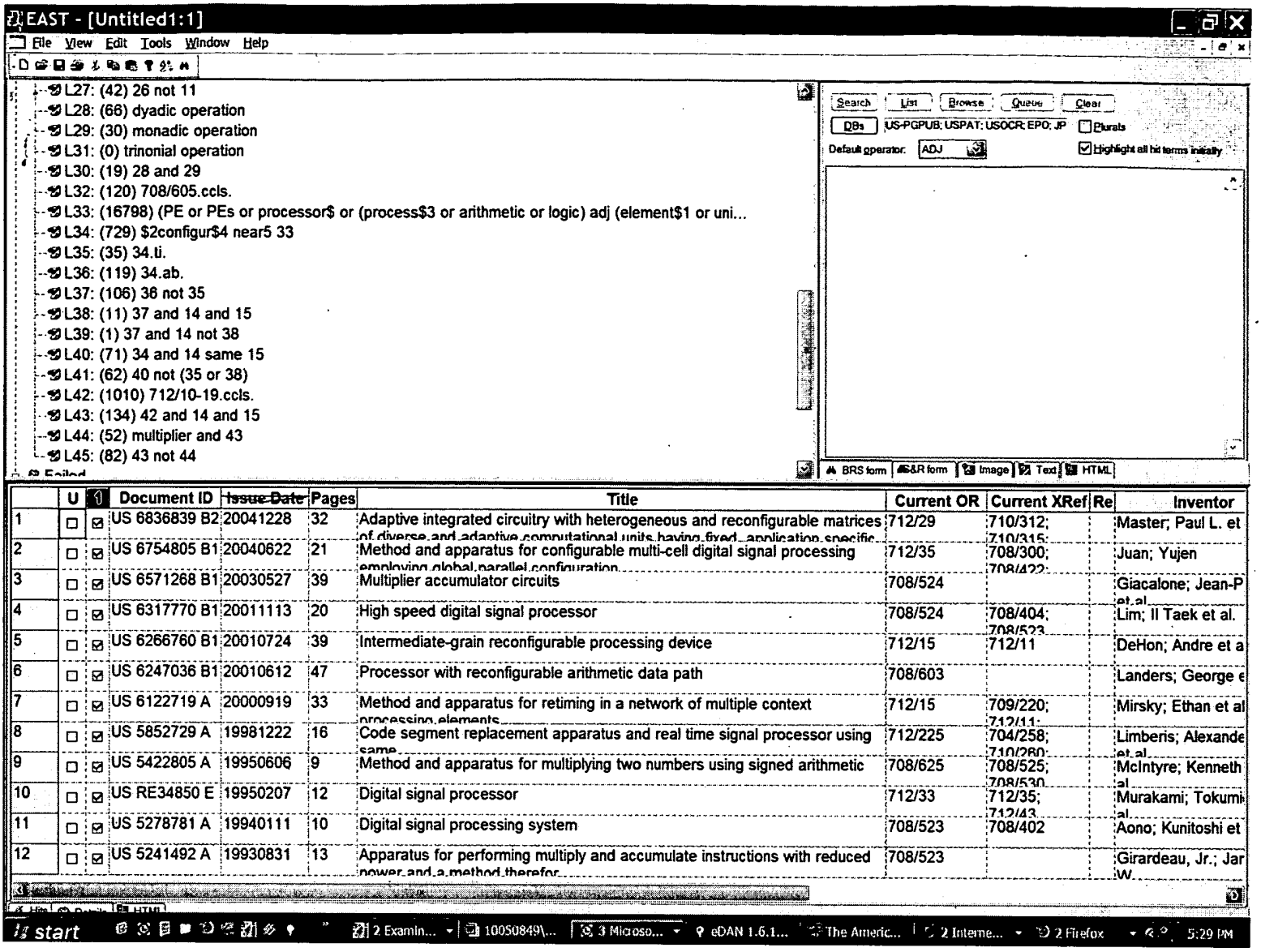

	U		Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re	Inventor
1	☐	☑	US 6836839 B2	20041228	32	Adaptive integrated circuitry with heterogeneous and reconfigurable matrices of diverse and adaptive computational units having fixed, application specific	712/29	710/312; 710/315;		Master; Paul L. et
2	☐	☑	US 6754805 B1	20040622	21	Method and apparatus for configurable multi-cell digital signal processing employing global parallel configuration	712/35	708/300; 708/422;		Juan; Yujen
3	☐	☑	US 6571268 B1	20030527	39	Multiplier accumulator circuits	708/524			Giacalone; Jean-P et al.
4	☐	☑	US 6317770 B1	20011113	20	High speed digital signal processor	708/524	708/404; 708/523		Lim; Il Taek et al.
5	☐	☑	US 6266760 B1	20010724	39	Intermediate-grain reconfigurable processing device	712/15	712/11		DeHon; Andre et a
6	☐	☑	US 6247036 B1	20010612	47	Processor with reconfigurable arithmetic data path	708/603			Landers; George e
7	☐	☑	US 6122719 A	20000919	33	Method and apparatus for retiming in a network of multiple context processing elements	712/15	709/220; 712/11;		Mirsky; Ethan et al
8	☐	☑	US 5852729 A	19981222	16	Code segment replacement apparatus and real time signal processor using same	712/225	704/258; 710/260;		Limberis; Alexande et al.
9	☐	☑	US 5422805 A	19950606	9	Method and apparatus for multiplying two numbers using signed arithmetic	708/625	708/525; 708/530		McIntyre; Kenneth al.
10	☐	☑	US RE34850 E	19950207	12	Digital signal processor	712/33	712/35; 712/43		Murakami; Tokumi al.
11	☐	☑	US 5278781 A	19940111	10	Digital signal processing system	708/523	708/402		Aono; Kunitoshi et
12	☐	☑	US 5241492 A	19930831	13	Apparatus for performing multiply and accumulate instructions with reduced power and a method therefor	708/523			Girardeau, Jr.; Jar W.